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by Chandrakasan, A.; Brodersen,  
R. W.;  
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## » Key

IEEE JNL IEEE Journal or Magazine  
 IEE JNL IEE Journal or Magazine  
 IEEE CNF IEEE Conference Proceeding  
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 IEEE STD IEEE Standard

- ☐ 1. **Power performance with gated clocks of a pipelined Cordic core**  
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Volume 2, 21-24 Oct. 2003 Page(s):1226 - 1230 Vol.2  
[AbstractPlus](#) | Full Text: [PDF\(391 KB\)](#) IEEE CNF  
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- ☐ 2. **Automatic insertion of gated clocks at register transfer level**  
Raghavan, N.; Akella, V.; Bakshi, S.;  
[VLSI Design, 1999. Proceedings. Twelfth International Conference On](#)  
7-10 Jan. 1999 Page(s):48 - 54  
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- ☐ 3. **Individual flip-flops with gated clocks for low power datapaths**  
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[Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on \[see also](#)  
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Volume 44, Issue 6, June 1997 Page(s):507 - 516  
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- ☐ 4. **Clock-gating and its application to low power design of sequential circuits**  
Qing Wu; Pedram, M.; Xunwei Wu;  
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Volume 47, Issue 3, March 2000 Page(s):415 - 420  
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5-8 May 1997 Page(s):479 - 482  
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